ISSN: 2277-9655
Impact Factor: 4.116

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

DESIGN AND DEVELOPMENT OF HYBRID MAC BASED ON CSCS

Annapurna Nand Tiwari*, Sourabh Sharma
* M-tech VLSI scholar Trinity institute of technology & research Bhopal, Mp India
Asst. Professor EC Dept.

DOI: 10.5281/zenodo.59642

ABSTRACT

FPGA based MAC has evolved into significant research field within engineering that encompasses the science of signal processing for developing a real-time digital analysis system. Due to the dynamic nature of applications, the MAC unit should offer low processing time and high resource optimization. In this paper, we propose novel multiplier-accumulator (MAC) hybrid architecture based on CSA with focus on development and advancement involving image/video processing based algorithms and other digital constraints. Many of the existing approaches rely on basic factor multiplication and accumulation as separate entities which would increasing the resources and time. An essential factor in effective design of novel MAC unit is the incorporation of multiplication and accumulation as single entity with accuracy and reduced cost. Further, application requires the minimum possible delay based on well defined principles. Unfortunately, MAC based on the existing approaches has high delay due to accumulator despite the large scale research and models. Henceforth, we incorporated Carry Save Adder (CSA) technique along with several parametric constraints to ensure the feasibility, effectiveness and efficiency of the proposed framework in comparison with the existing methods.

The novel structure of CSA exploits the radix-2 based 1's complement with benefits of altered Booth's Algorithm that address the sign expansion while minimizing the bits requirement based on operation constraints. The simulations analysis was carried out using ModelSim for conceptual analysis and Xilinx for feasibility analysis of the concept.

INTRODUCTION

"Electronic FPGA engineering" has become the most popular engineering discipline within a short panel time. Fundamentally this engineering discipline deals with the best practice for developing FPGA hardware based systems that refines the MOORE's LAW with a wide range of systems. Most of the world is dependent upon hardware based systems that are differentiated based on the resources, architecture, power dissipation, and computational time [1]. FPGA based MAC has evolved into significant research field within engineering that encompasses the science of signal processing for developing a real-time digital analysis system. Due to the dynamic nature of applications, the MAC unit should offer low processing time and high resource optimization with focus on development and advancement involving image/video processing based algorithms and other digital constraints. The FPGA architecture of the MAC is primary factor for righteous real-time of an application development phase as there is significant complexity and resources attached.

In the era of digital revolution, advancements in digital-media, network protocols, high speed transmission of digital information has created the need for real-time digital analysis. There has been a significant research progress in the area of real-time signal processing with applications ranging from filtering to pattern recognition. The most common and basic block that needs to be incorporated for any digital analysis would be ALU's, adder and multiplier.

This fact signifies the predominance of FPGA on hardware design activities. In general, these designs will be developed with series of different activities which need to be carried out simultaneously. The set of engineering frame work activities consists of various tasks like requirement design, resource allocation, and feasibility verification using

VHDL/Verilog, power/resource estimation [1]. Most of the present industrial clients are having conflicting demands about computation time, power dissipation factor, and architecture quality. These demands are really troubling the present industry. This is a serious need to think much about this situation in order to overcome the challenges arise due to conflicting demands.

To deal with the above challenges proper care should be taken while designing with reference computation time, power dissipation factor, and architecture quality. Hence my research work was focused more upon developing an innovative Multiplier-Accumulator (MAC) schematic which should aid the engineers to develop systems which reduced delay thus minimizing power requirement which ultimately minimizes the computation cost while offering improved architecture [2]. To gain extensive knowledge about these models, I reviewed many research publications and few text books related to the latest updates of multipliers, accumulators, and Multiplier-Accumulators (MAC).

Hardware engineering is a science that estimates the minimum possible resources and power dissipation considered necessary for the design and development of a system in concern. The inexactness of this development cost and overall power estimation is the main cause for the significant research and frustration of many organizations [1]. In recent years, various frameworks were introduced for cost effective (i.e. minimum delay) based architecture of different logical operational units necessary for various applications; unfortunately their efficiency is very low which includes high power dissipation, complex models and larger size. Due to rapid developments in image processing applications and real-time constraints Fast multipliers are evolving into integral part of various DSP systems [3].

The major problem regarding the development of fast multipliers lies with speed of accurate estimation and the sheer size of system which includes the use optimized resources, location of power source, logical units defined as metrics and the duration to complete delay. In general, it is commonly accepted fact that delay plays a prominent role in assessing the effectiveness of the system followed by the size and cost of the hardware. Unfortunately, these frameworks does not focus on the vital issues as it allows the enhancement of effective design which of great importance in digital signal processing application most in multimedia based applications (both offline and real-time). Since the multiplication is a basic operation that includes other basic arithmetic units such as addition, and/or subtraction, and shift operations in sequential and repetitive manner. We firmly believed that any repetitive logic could be designed in faster manner with limited use of resources that further reduces the power dissipation.

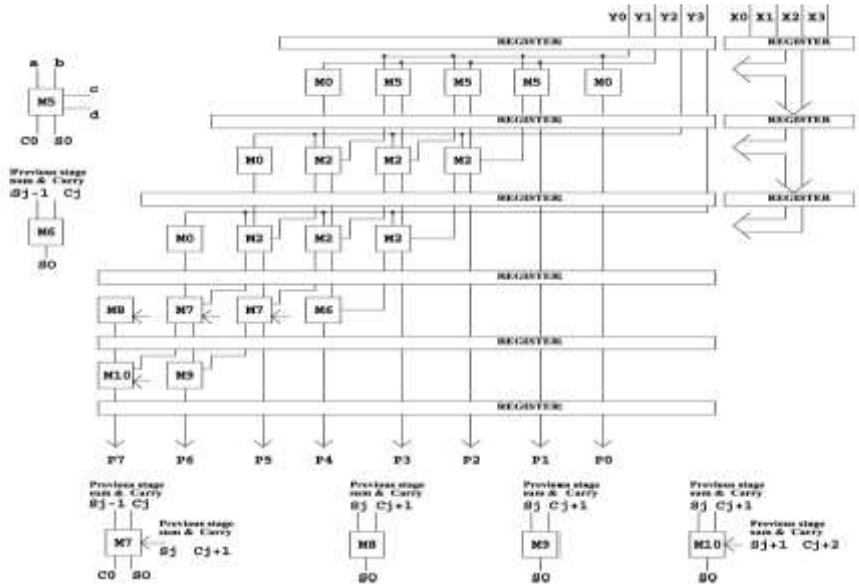

Figure 1. Basic block diagram of multiplication block

It is evident that the principle behind multiplication is technically a two-stage i.e. estimation of partial products and accumulation of the shifted partial products. It is evident that more than one approach is essential for successive additions so that there is a meaningful resource available for the shifted partial product estimation of the accurate

product that is critical for unique application. The designed architecture should ensure that 'multiplier' is adaptive shifted so as the gates receives the assigned bit of the 'multiplicand' which is vital aspect for enhancing and accurate estimation of the MAC system. Any multiplication must be carried out in a more diligently as it is a multi-operand operation. It is defined by set of executable arithmetic which performs a computational complex problem in an optimum manner as per the application requirement. Hence, there is concern of delayed response after each operation as gated instance of the multiplicand must all be in the same column of the shifted partial product matrix as they added to form the product bit for the particular form as presented in the figure 1.

Table 1: Varying Levels of complexity for evaluation of Hardware design and application

Level 1	Mathematical approaches (+/-)
	Boolean approaches
	Relational operation for data analysis
Level 2	Simple mathematical calculations (* / %)
	Simple interrelated approaches
	Relational operation for multi-dimensional data analysis
Level 3	Mathematical approaches
	Complex interrelated approaches
	Complex relational operation for multi-dimensional data analysis
	Analysis of data parameter and software requirements
Level 4	Complex mathematical approaches such as differential/integral based expression
	Complex logical operations based on soft-computing
	A complex combination of Boolean and Mathematical approaches
	Illustration and analysis of obscure operation
Level 5	Real-time data analysis
	Storage and offline processing by determining the priority
	Complex listing and queuing approaches

The primary steps in any process were to comprehend, evaluate, analyze and characterize the architecture of the system based on the requirement and application in which it would be incorporated. [4]. When proposed architecture of the hardware is insufficient or when the performance of hardware is limited then more often we alter the programming logic design to ensure proper working of the system as expected. To extend the multiplication to both signed and unsigned numbers, a convenient number system would be the representation of numbers in two's complement format [5]. As discussed, multiplication is a sequence of repetitive additions that generates a partial product at each stage of the operation. Multiplication is the popular eminent algorithmic frameworks that are commonly employed between two operands that can be viewed as two stage analysis as presented below [3-5]

1. Stage 1: Partial products between elements of the operands in consideration (for integers it become twice the size)
2. Stage 2: Accumulates these partial products and adds them but the repetitive addition has a significant delay. Henceforth focus has been shifted to positional analysis.

In this paper, we present a novel architecture for the Multiplier-Accumulator (MAC) Unit which, is predominantly used in several Multi-media processing based applications. In brief the proposed MAC algorithm system is based on operational manner of radix-4 algorithm incorporated with a vital functionality which defines the independence of the design focused Multiplier along with 34-bit CSA based on what it offers and how well it can be used to improve speed by minimizing the delay. In addition, it is also the parameter that ensures compatibility and transition from one

platform to another i.e. MIPS was implemented as micro processors and permitted high performance pipeline implementations through the use of their simple register oriented instruction sets.

LITERATURE SURVEY

In this section, we discuss various existing logical units (adder, subtractor, multiplier and accumulator) systems for digital applications while analyzing their drawbacks and advantages. Within the field of engineering, VLSI has evolved into an important and complex task in assessment of the feasibility of the hardware as it is vital in precise analysis of required operations and resources required in precise manner for the application. Several issues that plague the progress of the effort are the common understanding which it very complex and highly improbable to precisely assess the entire architecture from design to development to improve the delay, cost while maintaining the limited size of the system [4].

Due to the constant exploration within the field of semiconductor and introduction of nano-technology, there are several commonly used approaches were proposed for various classes of applications as presented in table 1. Based on the simulation results, we observe that each of existing approach has advantages as well as drawback in comparison with other approaches, as their advantages and limitations are often complimentary to each other. To understand the advantages and limitation of any method it is very important to know when you can use which method to estimate your delay [6-12]. The major issues of not improving delay of the logical unit can be credited to a several reasons of which the prime focus of this exposition is followed by below things [8]:

- The wrong scheduling of operand or non performing approach may be employed for shift the partial product
- The characteristic of the real-time problem for which the system is designed may not permit for improvement in delay and
- The constraints and process steps might repeatedly ignore several factors due to obscure design practice.

It is quite evident that the amount of background information on resource planning is essential for effective design in time is limited; all features as per the optimized requirement and various constraints needs to be considered. In addition, any system comes with considerable risks that can be mitigated as the most vital and critical attributes could have been assumed. But to the complexity increases with the decrease in size that could enhance the possibility of making the mistakes such as enhanced delay or power dissipation from one stage to another. Young et.al [7] introduced hybrid architecture of multiplier-and-accumulator (MAC) by exploiting both multiplier and accumulator with a carry save adder for high-speed arithmetic. Moreover, they synthesized over various sizes based on the benchmarked CMOS library. The simulation results prove that there was improvement in the delay, pipelining scheme, optimized resources in an effective manner. The proposed MAC was adaptable to various applications that encompass various signal processing applications. Vasant B.D et.al [8] introduced a schematic that addresses low power consumption and stratifies the necessary constraints of real-time applications. They exploit Booth algorithm in the architectural design of the system to address that commonly know limitations such as the enhanced area, resources and delay.

Jagadeesh.s et.al [9] developed a hybrid architecture of MAC for real-time digital signal processing applications that needs high-speed arithmetic. The efficiency of the proposed system was enhanced by carry save adder (CSA) and exploiting SPST (Spurious Power Suppression Technique). It is evident from the simulation results that the Booth Multiplier would enhance the performance by improving computation speed of Multipliers and SPST reduces the power consumption. Sathish, M. M., and Sailaja, M. [10] introduces high-speed arithmetic MAC architecture by exploiting the advantages of multiplier and accumulator in a single phase to improve the overall performance of the MAC. It is general understanding that the accumulator carries the maximum delay that arises in MAC but due to the incorporation CSA tree structure that utilizes 1's-complement-based radix-2 modified Booth's algorithm (MBA) along with the other modified features offer superior functionalities that could helpful for various real-time applications. Tsoumanis, K. et.al. [11] presented an optimized design of fused Add-Multiply (FAM) that forms a part of new ALU development that is used effectively as a local complex arithmetic operator for diverse DSP applications. This strategy examines the operator that exploits Modified Booth technique to evaluate the direct sum between 2 numbers. Comparing them with the FAM designs which use existing recoding schemes, the proposed technique yields considerable reductions in terms of critical delay, hardware complexity and power consumption of the FAM unit. Mactaggart, I. R. et.al. [12] signified the importance of the parallel-data arithmetic computations over various

ISSN: 2277-9655
Impact Factor: 4.116

distributed arithmetic technique. Several other designs and structures they applications and characteristics are presented by several researchers [13-18].

The standard set extension of the multiplier framework for creating the initial direct structure that offers perspective apart from traditional systems which are essentially instruments to comprehend the growing requirement in DSP applications. The addition of partial products based on encoding framework should be as parallel as possible to minimize the delay that propagates the entire operation that depends on number of inputs. Ant brilliant structure is prepared to process completely operations that are well defined and authentic i.e. to enhance the computational speed of a multiplier by reducing the delay and/or the number of the partial products.

MULTIPLIER AND ACCUMULATOR (MAC)

A multiplier between any two binary numbers involves two main operations i.e. shift and add. Unfortunately, each of the product obtain at a location needs to be saved till the corresponding partial product is available thus increasing the number operations as well as delay. In fact the modern multipliers operation can be expresses with three major components as presented in figure 2 i.e. booth encoding, partial product summation and final addition that is calculated by the addition of corresponding sum and carry. But MAC includes a major fourth step of accumulation, as shown in figure. 2, which shows the operational steps in explicit manner.

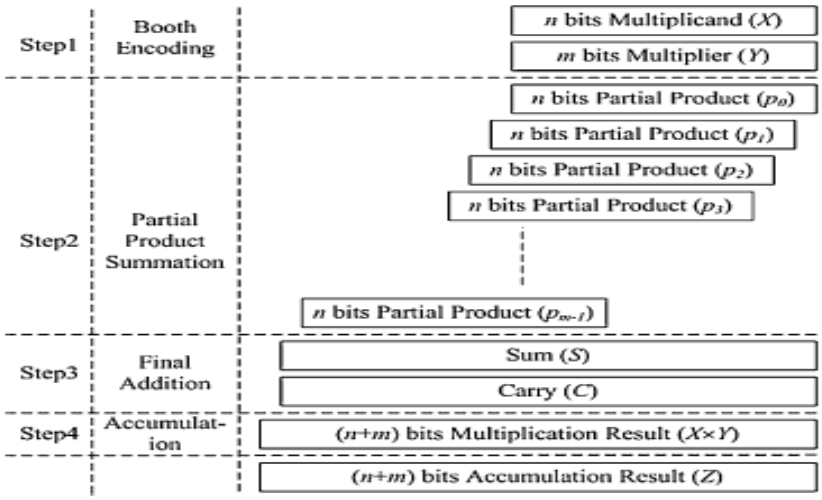

Figure 2. Basic Steps of MAC

To the unclearness of MAC architecture and expression in creating framework, the pure multiplication operation is extremely useful. Significantly to tackle the ambiguities concerned within the general MAC architecture, method of multiplying two unsigned values X and Y could be executed. The general, N-bit 2's complement is

$$X = -2^{N-1}x_{N-1} + \sum_{i=0}^{N-2} x_i 2^i, \qquad x_i \in 0, 1.$$

Upon expanding to base-4 type based on sign form, we have

$$X = \sum_{i=0}^{N/2-1} d_i 4_i$$

$$d_i = -2x_{2i+1} + x_{2i} + x_{2i-1}.$$

Mathematically multiplication is defined as

$$X \times Y = \sum_{i=0}^{N/2-1} d_i 2^{2i} Y.$$

ISSN: 2277-9655
Impact Factor: 4.116

And MAC is defined by the expression

$$P = X \times Y + Z = \sum_{i=0}^{N/2-1} d_i 2^i Y + \sum_{j=0}^{2N-1} z_i 2^i.$$

Each term in the expression i.e. "Y+Z" and "X*(Y+Z)" are independently evaluated [6]. The number of partial products obtained in the multiplier depends on the number of bits multiplied. The delay and computation time required for the serial addition would be significant that could be addressed by incorporating the benefits of the Booth techniques by exploiting radix-2 approach. Upon applying this approach the number of operations required for partial product is minimized to half. The total schematic of the entire process based on its operations employed at modular level is exploited at various stages of pipeline design as illustrated in figure 3.

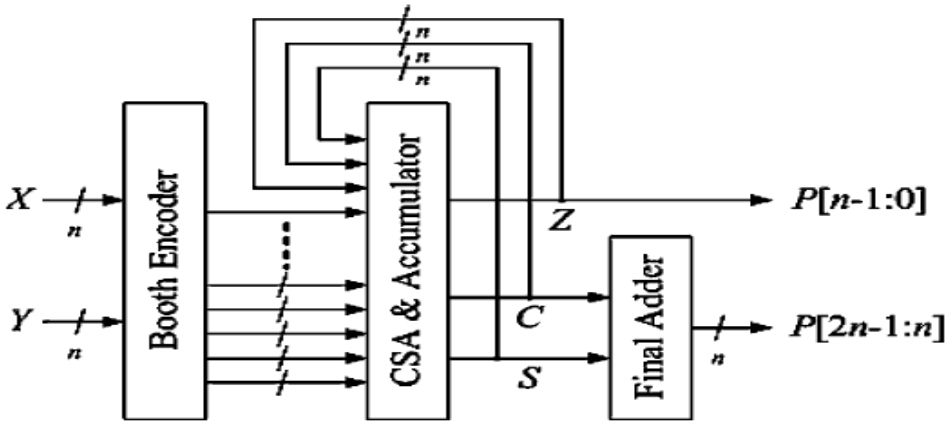

Figure 3. Pipeline design illustrating various stages of MAC in two N-bit multiplications

It is evident that there is a significant relation between inputs, partial products and final adder that needs to be balanced in order to have an optimum delay for the proposed MAC. Any change in one of the factors would results a corresponding impact on other two attributes. In addition, to increase the output rate when pipelining is applied, the outputs sum and carry from each CSA get accumulated which in turn becomes the input of the final adder. Due to this feedback analysis of both sum and carry, the number of inputs to CSA increases, compared to the standard design and [17].

MAC Unit

It is well documented MAC consists of prime components i.e. multiplier, adder, and an accumulator based on the selection of scale drivers have an impact on the delay and detail deliberations are studied in coming sections and chapters. Therefore, each scale driver taken depends on various applications factors and features such "Carry- Select" or "Carry-Save" adder is incorporated for DSP applications wherein computation speed is of utmost importance. An effective assessment helps like parallel array multiplier could be exploited as multiplier.

The implementation vagueness covers the inputs for the MAC to multiplication segment is completed and offers result to adder and based on the operational factors it accumulates the result into a memory location. To multiply the values of A and B, Modified Booth multiplier is used instead of conventional multiplier because Modified Booth multiplier can increase the MAC unit design speed and reduce multiplication complexity. This MAC unit has 34 bit output and its operation is to add repeatedly the multiplication results. Power delay product is calculated by multiplying the power consumption result with the time delay.

A radix-4 modified Booth's algorithm

Booth's technique powerful approach to enhance MAC performance that depends largely on partial products and accumulator features by minimizing partial products. The radix-4 offers the major benefits i.e. the in conventional

ISSN: 2277-9655
Impact Factor: 4.116

process 17 partial products needs to be addressed for two 16-bits signed or unsigned multiplication whereas Radix-4 has a 3x term needs to be employed encoding processing. At any given instance, this radix-4 modified Booth's factor is combination 3 bits grouping inputs for the multiplier that overlaps and has half of the partial products. Hence the Booth's radix-4 significantly enhances the computation speed of the system with the basic steps discussed in detail [19].

Sign or zero extension

This is an important factor that determines the maximum extent of the MAC application and performance along with its functional durability. In case of MAC, signed or unsigned multiplication is supported which produces final result up to 64-bits that are stored in two 32-bit register. The impact of the application failure is insignificant as 17 partial products are generated. Here is an example of signed and unsigned multiplication.

signed (-1 x -1 = 1)						
x		(1)	1	1	1	
y	×	(1)	1	1	1	(0)
0	0	0	0	0	1	1x
0	0	0	0	0		0x
0	0	0	0	0	1	1_{dec}

unsigned (7 x 7 = 49)						
x		(0)	1	1	1	
y	×	(0)	1	1	1	(0)
1	1	1	0	0	1	-x
1	1	1	0			+2x
1	1	0	0	0	1	49_{dec}

Carry Save Adder (CSA)

When three or more operands are to be added simultaneously using two operand adders, the time consuming carry propagation must be repeated several times. If the number of operands is 'k', then carries have to propagate (k-1) times. In the carry save addition, we let the carry propagate only in the last step, while in all the other steps we generate the partial sum and sequence of carries separately. A CSA is capable of reducing the number of operands to be added from 3 to 2 without any carry propagation. A CSA can be implemented in different ways. In the simplest implementation, the basic element of carry save adder is the combination of two half adders or 1 bit full adder.

PROPOSED DESIGN

The major problem regarding the MAC lies with delay and the duration to complete the operation as real-time applications needs high speed and minimum delay. In terms of hardware engineering, the measure of hardware design quality and feasibility can be expressed as a function of the issues related with the product i.e. is it has minimum delay, size, and power consumption and so on. With significant rise in the demand of the quality in multipliers, MAC is becoming a popular method to address such issues of DSP system. The MAC technique can be viewed as collection of independent heterogeneous sub-modules for practical advantage to mark each module individually based on the characteristic and functionality. The marking of the individual circuit design to investigate various Pipelined multiplier/accumulator to achieve low power consumption is prime motivation of the investigation. This helps us to investigate and mark every module in MAC in one run; a conventional MAC contains the sum of the previous consecutive products as given by expression below:

$$F = \Sigma A i Bi$$

The major factor of this research is to enhance the speed of the MAC unit, while minimizing the power consumption and delay. In a pipelined MAC circuit, the delay of pipeline stage is the delay of a 1-bit full adder. Estimating this delay will assist in identifying the overall delay of the pipelined MAC. The feasibility study of the entire MAC depends on three factors i.e. size, power and delay which are calculated for a full adder, thus it helps us in designing a low powered pipelined MAC unit.

ISSN: 2277-9655
Impact Factor: 4.116

Proposed Encoder Design

In this section, we propose new hybrid multipliers that consolidate various attributes required for DSP based systems. It is evident that conventional multiplier utilizes a combination of addition, subtraction, and shift operations to evaluation and repeated in case of large bits. Each technique has several advantages and corresponding limitations, so to obtain a precise evaluation a partial product is generated at end of each stage of adder. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content. The entire process complex, henceforth the multipliers are mostly decomposed into two parts that benefits and optimizes good hardware design fold i.e. evaluation of partial products and accumulation of the shifted partial products. Booth algorithm is a high-speed multiplication technique that allows use of parallel counters for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. By incorporating the radix-4 technique it is quite possible to reduce the number of partial products by half. One of the major advantage of the MBA if that its operation speed is faster than of array multiplier the basic block diagram is presented in the figure 5. It is evident that shifting and adding for each multiplier column and multiply by 1 or 0 provides a similar result wherein every second column is multiplied by ±1, ±2, or 0. Furthermore, essential and meaningful available resources (power and delay) are preserved [21]. In addition, a group of three bit-blocks are generated with a constraint that each bit-block overlap the prior one by 1-bit.

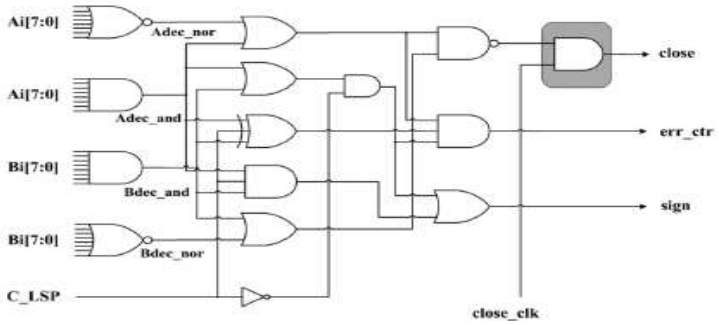

Figure 4. The basic block diagram of MBA

Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a certain operation on the multiplicand, X.

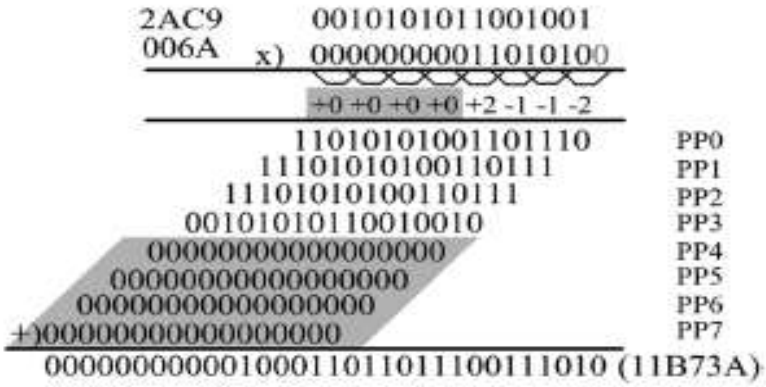

Figure.5 Illustration of multiplication using modified Booth encoding

With constant development and evolution within the research area of software engineering there is a significant rise in cost assessment techniques that focus of duration and coding length. Radix-4 Modified Booth algorithm is incorporated to minimize the partial products by half. In addition, a significant number of outputs are zeros hence these computations can be neglected which reduces the power consumption. When the operand besides the Booth

ISSN: 2277-9655
Impact Factor: 4.116

encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree

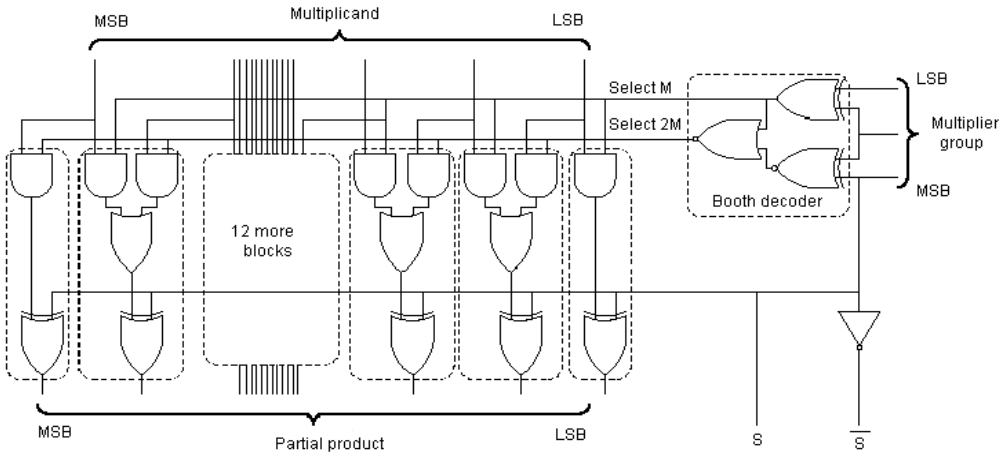

Figure. 6 Booth partial product selector logic

Partial product

The basic block diagram for the Booth encoder of the proposed system that incorporates the selector logic mechanism is presented in the Figure 6. As explained in earlier section, we focus on minimizing the number of partial products generated for capitalize the delay generated by the accumulator block. The coding is performed over signed and unsigned bits.

Proposed Encoder

In this section, we present the proposed system that would enhance the robustness along with the speed of Multiplication algorithm. We decompose the multiplication into three major phases:

1) Generation of the partial products;
2) Addition of these products based on the constraints proposed
3) Computation of the output by adding final rows.

By analysis of the each phase based on MBA the number of partial products could be reduced to half in the initial phases just improving the alternate phases. Modified Booth Encoding (MBE) is a popular scheme of coding data within the digital domain in an effective manner.

SPST

The SPST involves the calculation of the "best basis", which is a minimal representation if the relative to a particular function. The basic SPST can be viewed as a technique that can dramatically reduce the power dissipation of combinational VLSI designs for multimedia/DSP purposes. The next level of the tree is the result of one step and subsequent levels in the tree are constructed by recursively applying partial product addition from previous transform step. The 1st case illustrates a transient state in which the spurious transitions of carry signals occur in the MSP though the final result of the MSP are unchanged. The 2nd and the 3rd cases describe the situations of one negative operand adding another positive operand without and with carry from LSP, respectively. Moreover, the 4th and the 5th cases respectively demonstrate the addition of two negative operands without and with carry-in from LSP.

AMSP = A[15:8]; BMSP = B[15:8] ;
Aand = A[15] A[14] A[8];
Band = B[15] B[14] B[8];]

$$A_{nor} = \overline{A[15] + A[14] + A[13] + \cdots + A[8]};$$

$$B_{nor} = \overline{B[15] + B[14] + B[13] + \cdots + B[8]};$$

$$Close = \overline{(Aand + Anar) \cdot (Band + Bnar)};$$

ISSN: 2277-9655
Impact Factor: 4.116

Latches implemented by simple AND gates are used to control the input data of the MSP. When the MSP is necessary, the input data of MSP remain the same as usual, while the MSP is negligible, the input data of the MSP become zeros to avoid switching power consumption. Further to decrease the glitch signals occurred in the cascaded circuits which are usually adopted in VLSI architectures designed for video coding.

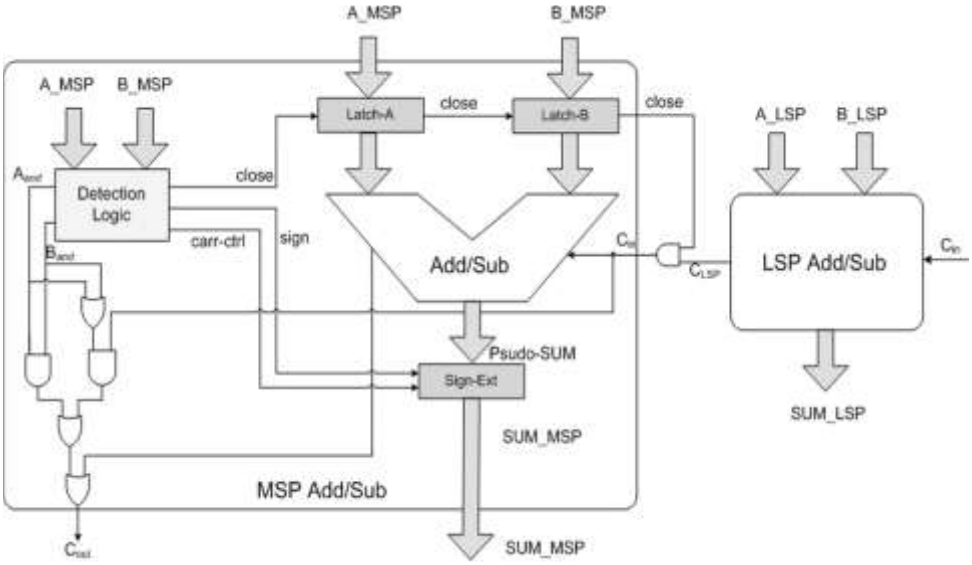

Figure 7. 16-bit adder/subtractor design example adopting the proposed SPST.

SIMULATION RESULTS

In this section, the simulations results of proposed multiplier-accumulator (MAC) that offers improved delay and speed for real-time digital signal processing (DSP) applications are presented. Computer simulations were simulated using ModelSim for conceptual analysis and Xilinx for feasibility analysis of the concept.

Phase 1: Analysis

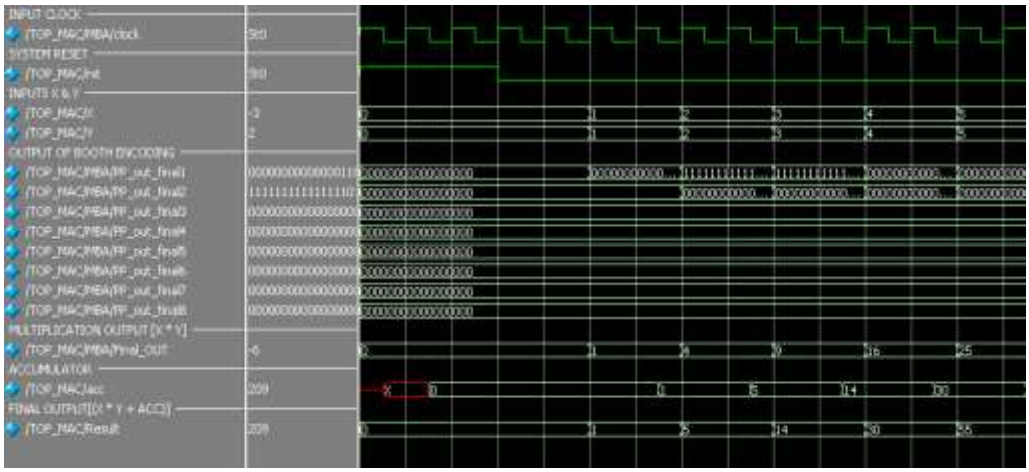

Figure 8. Simulation analysis of the proposed MAC

Phase 2: Design Flow

Initial investigation to simulation analysis, was based on the randomness of the process in consideration. Hence, to measure the robustness of the proposed system, we need to evaluate the design flow of proposed FPGA architecture of the proposed system. The FPGA offers inter connected logic blocks with a two dimensional arrays wherein both are programmable. Logic blocks are programmed to implement a desired function and interconnect are programmed

using the switch boxes to connect the logic blocks. Our basic metric set of the hardware structure focuses on size (area), computation time, power dissipation and unforeseen defects for the feasibility of the system, and optimized design. In Xilinx case methods calibrate the model to specific environment and/or project time circumstances based on logic blocks that consist of Look-up-table and Flip-Flop. Unfortunately, Look-up-table based methods are highly correlated to the several parameters in above discussion which lead to mixed results. The proposed method uses a combination of registered and non-registered outputs from the Look-up-tables to offer robust, efficient, and consistent results.

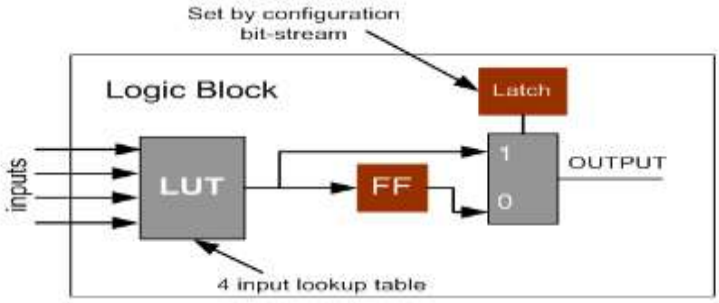

Figure 9. below shows a 4-input LUT based implementation of logic block

Phase 3: Synthesis Result

The alternative analysis is created RTL methodology, wherever it imparts their seeing concerning endeavor house. With proposed algorithm getting to be a lot of dynamic, self-ruling we evaluate the synthesis analysis using Xilinx ISE tool and other concerns are addressed. In this phase, gate level based net-list is generated based on the proposed system RTL model that is mapped with SPL. The proposed MAC design is synthesized on a Spartan 3E.

Device utilization summary:

mac1 Project Status			
Project File:	mac1.ise	**Current State:**	Synthesized
Module Name:	top_tst	**• Errors:**	No Errors
Target Device:	xc3s500e-4fg320	**• Warnings:**	22 Warnings
Product Version:	ISE 10.1 - Foundation Simulator	**• Routing Results:**	
Design Goal:	Balanced	**• Timing Constraints:**	
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	

mac1 Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1182	4656	25%
Number of Slice Flip Flops	678	9312	7%
Number of 4 input LUTs	1863	9312	20%
Number of bonded IOBs	1	232	0%
Number of BRAMs	4	20	20%
Number of GCLKs	2	24	8%

In timing summery, details regarding time period and frequency is shown are approximate while synthesize. After place and routing is over, we get the exact timing summery. Hence the maximum operating frequency of this synthesized design is given as 86.987 MHz and the minimum period as 11.496 ns. Here, OFFSET IN is the minimum input arrival time before clock and OFFSET OUT is maximum output required time after clock.

CONCLUSION

In this paper, we proposed novel multiplier-accumulator (MAC) hybrid architecture based on CSA with focus on development and advancement involving image/video processing based algorithms and other digital constraints. It has been verified that the essential factor in effective design of novel MAC unit is the incorporation of multiplication and accumulation as single entity with accuracy and reduced cost. We incorporated Carry Save Adder (CSA) technique

along with several parametric constraints to ensure the feasibility, effectiveness and efficiency of the proposed framework in comparison with the existing methods.

- The developed MAC design is modelled and is simulated using the Modelsim which shows promising results in delay and area issues.
- the simulation results are discussed by considering different cases that show the proposed system is applicable for real time applications and speedy DSP application based on Design flow analysis.
- The RTL model is synthesized using the Xilinx tool in Spartan 3E and their synthesis results were discussed with the help of generated reports show that resources employed is reduced, delay has been addresses and computation time of the proposed system is high.
- The novel structure of CSA exploiting the radix-4 based 1's complement with benefits of Modified Booth's Algorithm (MBA) addressed the sign expansion in an effective manner while minimizing the bits requirement based on operation constraints is feasible.

REFERENCES

[1] Barkan, M. (1988). U.S. Patent No. 4,736,335. Washington, DC: U.S. Patent and Trademark Office
[2] K. S. Yeo, K. Roy, Low Voltage Low Power VLSI Subsystems, Book, Mc Graw Hill Professional Engineering, 2005
[3] S. D. Brown, Fundamentals of Digital Logic with Verilog Design, 2nd Edition, Book Mcgraw Hill, 2007
[4] M. Mano, Digital Circuits and Systems, Prentice-Hal, 2011
[5] Khan, I., Shah, S., & Kapse, V. (2015, January). Quick Review on Multiplication Algorithm for Enhancing Efficiency of MAC Unit. In Proceedings of International Conference of Advance Research and Innovation (pp. 159-162).
[6] Swamy, K. N., & Suman, J. V. (2016). Design of Optimized Multiply Accumulate Unit Using EMBR Techniques for Low Power Applications. In Computational Intelligence in Data Mining—Volume 2 (pp. 315-323). Springer
[7] Seo, Y. H., & Kim, D. W. (2010). A new VLSI architecture of parallel multiplier–accumulator based on Radix-2 modified Booth algorithm. IEEE Transactions on very large scale integration (vlsi) systems, 18(2), 201-208.
[8] Vasant, B. D., & Sapkal, A. M. (2013). A NEW VLSI ARCHITECTURE OF PARALLEL MULTIPLIER ACCUMULATOR BASED ON RADIX-2 MODIFIED BOOTH ALGORITHM
[9] Jagadeesh, S., & Chary, S. V. (2012). Design of Parallel Multiplier–Accumulator Based on Radix-4 Modified Booth Algorithm with SPST.International Journalof Engineering Research and Application.
[10] Sathish, M. M., & Sailaja, M. VLSI architecture of parallel multiplier–accumulator based on radix-2 modified booth algorithm. International Journal of Electrical and Electronics Engineering (IJEEE), 1.
[11] Tsoumanis, K., Xydis, S., Efstathiou, C., Moschopoulos, N., & Pekmestzi, K. (2014). An optimized modified booth recoder for efficient design of the add-multiply operator. IEEE Transactions on Circuits and Systems I: Regular Papers, 61(4), 1133-1143.
[12] Mactaggart, I. R., & Jack, M. A. (1984). A single chip radix-2 FFT butterfly architecture using parallel data distributed arithmetic. IEEE journal of solid-state circuits, 19(3), 368-373.
[13] Swee, K. L. S., & Hiung, L. H. (2012, June). Performance comparison review of Radix-based multiplier designs. In Intelligent and Advanced Systems (ICIAS), 2012 4th International Conference on (Vol. 2, pp. 854-859). IEEE.
[14] Sasidharan, D. G., & Iyer, A. (2013). Comparison of Multipliers Based on Modified Booth Algorithm. International Journal of Engineering Research and Applications (IJERA) ISSN, 2248-9622.
[15] Babu, N. J., & Sarma, R. (2016). A Novel Low Power Multiply–Accumulate (MAC) Unit Design for Fixed Point Signed Numbers. In Artificial Intelligence and Evolutionary Computations in Engineering Systems (pp. 675-690). Springer
[16] Pedroni, V. A. (2013). Finite State Machines in Hardware: Theory and Design (with VHDL and SystemVerilog). The MIT Press
[17] Basha, S. S., & Jahangir, B. S. (2012). Design and implementation of radix-4 based high speed multiplier for alu's using minimal partial products.International Journal of Advances in Engineering and Technology, 4(1), 314-25.

[18] Goyal, R., Dey, A. K., & Gupta, N. (2015). U.S. Patent No. 8,933,731. Washington, DC: U.S. Patent and Trademark Office.
[19] Karthikeyan, K. V., Babu, R., Mathan, N., & Karthick, B. (2016). Performance analysis of an efficient MAC unit using CNTFET technology.Materials Today: Proceedings, 3(6), 2525-2531
[20] Parandeh-Afshar, H., Fakhraie, S. M., & Fatemi, O. (2010). Parallel merged multiplier–accumulator coprocessor optimized for digital filters. Computers & Electrical Engineering, 36(5), 864-873.
[21] Rajput, R. P., & Swamy, M. S. High Performance Iterative Pipelined Multiply and Accumulator for Signed-Unsigned Number
[22] Sharif, S. M., & Prasad, D. Y. V. Design of Optimized 64 Bit MAC Unit for DSP Applications.
[23] Kumar, R. V., & Kamala, J. (2012). High accuracy fixed width multipliers using modified booth algorithm. Procedia Engineering, 38, 2491-2498